AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Currently Amended) A digital circuit for shifting a frequency band of a signal vector to a predetermined frequency band, wherein the signal vector is determined by a pair of I (in-phase) and Q (quadrature) components on I-Q plane, comprising:

a control data generator for generating control data from a frequency difference between the frequency band and the predetermined frequency band including a phase data generator for generating phase data from the frequency difference;

a signal vector rotator for rotating the signal vector on the I-Q plane by an angle determined depending on the control data to produce an output signal vector in the predetermined frequency band;

an analog-to-digital converter for converting a received analog signal vector to the signal vector according to a predetermined sampling clock,

wherein the control data generator comprises:

a phase data generator for generating phase data from the frequency difference in synchronization with the predetermined sampling clock; and

a converter for converting the phase data to the control data consisting of a plurality of control bits ~~according to claim 2~~, and

wherein the signal vector rotator comprises:

a plurality of partial rotators which are connected in series in descending order of a rotation angle, wherein each of the partial rotators receives a different bit of the control bits of the control data and rotates an output of a previous stage by a predetermined angle depending on a corresponding control bit received from the converter.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Currently Amended) A digital circuit for shifting a plurality of frequency bands of input signal vectors to a predetermined center frequency band to produce an output signal vector for each frequency band, wherein each of the input signal vectors is determined by a pair of I (in-phase) and Q (quadrature) components on I-Q plane, comprising:

an analog-to-digital converter for converting analog signal vectors to the input signal vectors according to a predetermined sampling clock;

a control data generator for generating control data from a frequency difference between each of the plurality of frequency bands and the predetermined center frequency band including a phase data generator for generating phase data from the frequency difference;

a signal vector rotator corresponding to each of the plurality of frequency bands, for rotating the input signal vectors on the I-Q plane by an angle determined depending on corresponding control data to shift the frequency bands of the input signal vectors to the predetermined center frequency band;

a band-pass filter corresponding to the signal vector rotator, for receiving an output of the signal vector rotator and passing an output signal vector of the predetermined center frequency band;

wherein the control data generator comprises:

a phase data generator for generating phase data Φ from the frequency difference in synchronization with the predetermined sampling clock; and

a converter for converting the phase data Φ to the control data D consisting of a plurality of control bits D_k, where $-1 \leq k \leq m-2$ (m is a positive integer) ~~The digital circuit according to claim 6~~,

wherein the phase data generator generates the phase data Φ by computing an integral multiple of a unit angle Δ which is obtained from a frequency shift δ per period of the predetermined sampling clock, wherein the unit angle Δ is represented by $360° \times \delta$, wherein the frequency shift δ is obtained by dividing the frequency difference by a frequency of the predetermined sampling clock and is represented in form of $RN/2^m$ (RN is a rational number).

8. (Original) The digital circuit according to claim 7, wherein the converter performs a conversion operation according to the following steps:

Step 1) $k = -1$ and $\Phi_k = \Phi$;

Step 2) D_k = sign bit of Φ_k;

Step 3) if $k = m - 2$, then exit, else go to step 4);

Step 4) $\Phi_{k+1} = \Phi_k - \theta_k$ when $D_k = 0$, and

$\Phi_{k+1} = \Phi_k + \theta_k$ when $D_k = 1$, where $\theta_k = \arctan(2^{-k})$;

Step 5) $k = k + 1$; and

Step 6) go to step 3).

9. (Original) The digital circuit according to claim 8, wherein the signal vector rotator comprises:

a plurality of partial rotators R_k which are connected in series in descending order of a rotation angle, wherein the partial rotators R_k receive the control bits D_k, respectively, and each of the partial rotators R_k rotates an output of a previous stage R_{k-1} by a predetermined angle depending on a corresponding control bit received from the converter.

10. (Original) The digital circuit according to claim 9, wherein

a first partial rotator R_{-1} rotates an input signal vector (I_{in}, Q_{in}) by an angle θ_{-1} to produce a first output signal vector $(I_{out,-1}, Q_{out,-1})$ as follows:

$$I_{out,-1} = D_{-1} \times Q_{in}; \text{ and}$$

$$Q_{out,-1} = -D_{-1} \times I_{in},$$

each of partial rotators R_k $(0 \leq k \leq m-2)$ rotates an input signal vector $(I_{in,k}, Q_{in,k})$ by an angle θ_k to produce an output signal vector $(I_{out,k}, Q_{out,k})$ as follows:

$$I_{out,k} = I_{in,k} + 2^{-k} \times D_k \times Q_{in,k}; \text{ and}$$

$$Q_{out,k} = -2^{-k} \times D_k \times I_{in,k} + Q_{in,k},$$

where D_k uses numerical value representation such that a numerical value "1" is represented by a logical value "1" and a numerical value "-1" is represented by a logical value "0".

11. (Original) The digital circuit according to claim 9, wherein the signal vector rotator rotates an input signal vector (I_{in}, Q_{in}) having an absolute value Z_{in} by an angle Θ while the absolute value Z_{in} becomes Z_{out}, where Θ and Z_{out} are represented as follows:

$$\Theta = D_{-1} \times 90^{\circ} + \sum_{k=0}^{m-2} D_k \bullet \arctan(2^{-k}) \quad \textit{and}$$

$$Zout = \frac{Zin}{\prod_{k=0}^{m-2} \cos\theta_k} \quad .$$

12. (Canceled)

13. (Canceled)

14. (Canceled)